Abstracts

Simple and efficient full-wave modeling of electromagnetic coupling in realistic RF multilayer PCB layouts

M.R. Abdul-Gaffoor, H.K. Smith, A.A. Kishk and A.W. Glisson. "Simple and efficient full-wave modeling of electromagnetic coupling in realistic RF multilayer PCB layouts." 2002 Transactions on Microwave Theory and Techniques 50.6 (Jun. 2002 [T-MTT]): 1445-1457.

A simple method to model a printed circuit board (PCB) that takes advantage of the unique features found in PCBs is proposed. This method is capable of analyzing coupling between any nets in the entire multilayer PCB. Using the equivalence principle, the PCB is modeled as a cascade of parallel-plate waveguides with half-space regions residing above and below the PCB. Instead of formulating the problem in terms of electric currents in the horizontal metal layers, it is formulated using equivalent magnetic currents in the nonmetallic regions of layer interfaces. The equivalent magnetic currents at the dielectric interfaces are expressed in terms of the Rao-Wilton-Glisson (RWG) basis functions. The electric currents flowing on the vias inside dielectric layers are assumed constant in the vertical direction. These vertical electric currents radiate TEM modes in the parallel-plate environment. Integral equations based on simple parallel-plate and free-space Green's functions enforcing the boundary conditions are set up and solved using the method of moments (MoM). The equivalent magnetic currents in each layer interact with currents in the adjacent layers only, thereby resulting in a "chained-block-banded" matrix. Excitation is provided through ports defined at each pair of pads, or between a pad and nearby ground. These ports are located only on the top and the bottom layers of the PCB where the circuit components and integrated-circuit pins are mounted. Two different localized excitation schemes, one with a current loop injection and the other with a strip current excitation, are proposed. This formulation requires the computation of the MoM matrix only once per frequency for any number of ports. Further, the solution for only those unknown equivalent magnetic currents around the port regions is required to obtain the N-port impedance parameter characterization of the PCB. Consequently, a memory-efficient block matrix solution process can be used to solve problems of large size for a given memory. Simple and realistic examples are given to illustrate the applicability of this approach.

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